Time-Based ADCs

Michael Kalcher

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Time-Domain Signals

- VDSM technologies: may be beneficial to operate on time differences rather than voltages
- Time-domain signals:
  - Digital signal levels of $0\ \mathrm{V}$ and V_{DD}
  - Information stored in delay of transitions referred to reference signal (e.g. low jitter clock)
- Conversion from voltage to time domain necessary: Voltage-to-Time Converter (VTC), already includes sampling
- Instead of (conventional) ADC: Time-to-Digital Converter (TDC) for quantization

Time-Domain Analog-to-Digital Converter

Simplest time-based ADC:

- VTC in cascade with TDC

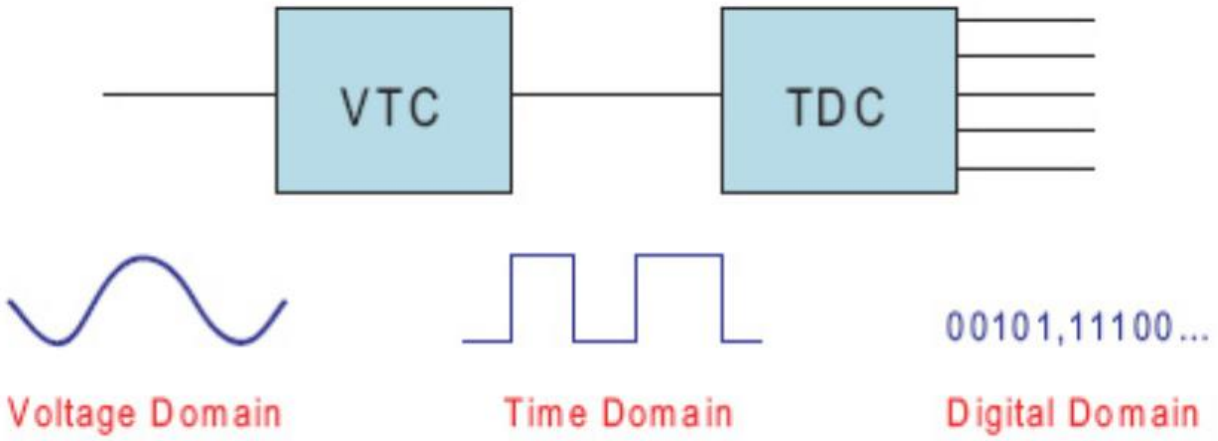
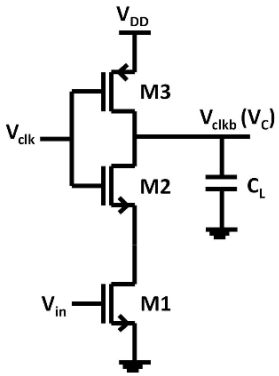


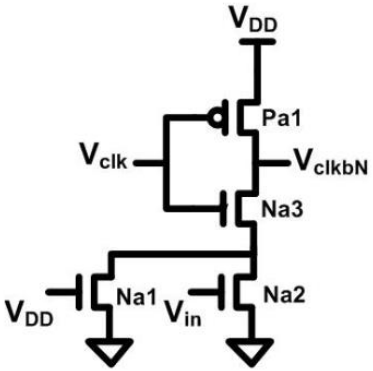
Image from [1]

Voltage-to-Time Converter

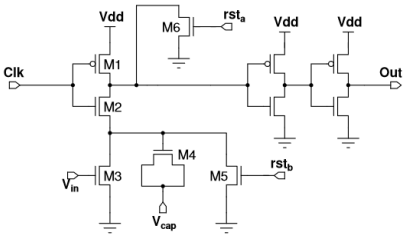
- Inherently sample the analog input signal
- Most high-speed topologies rely on current starved inverters
- Limited linearity, mostly limited to 4 or 5 bit



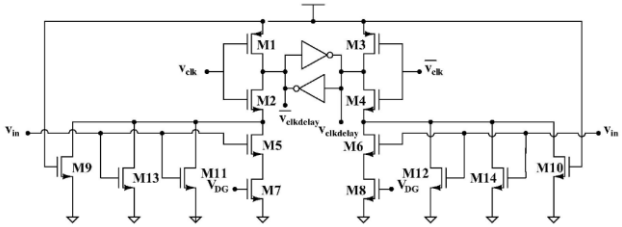
[1], [2]



[1]



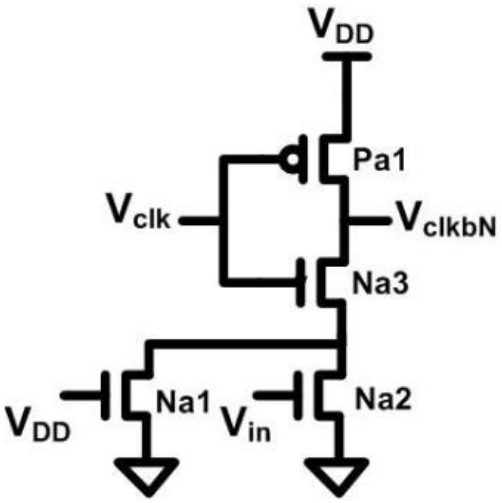
[3]



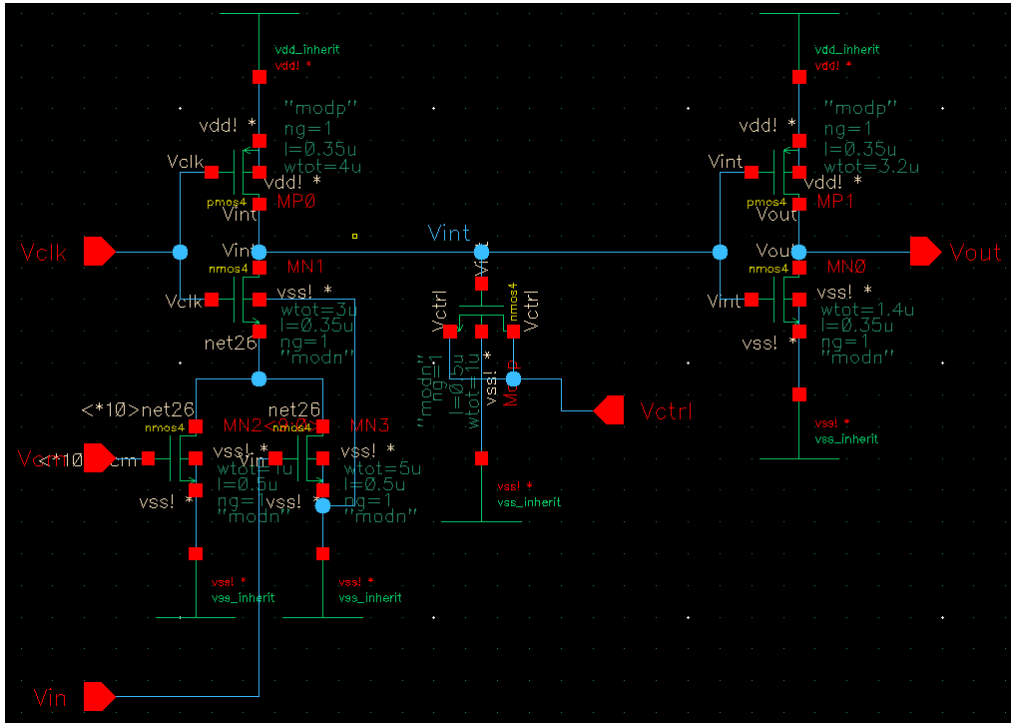
[2]

Voltage-to-Time Converter

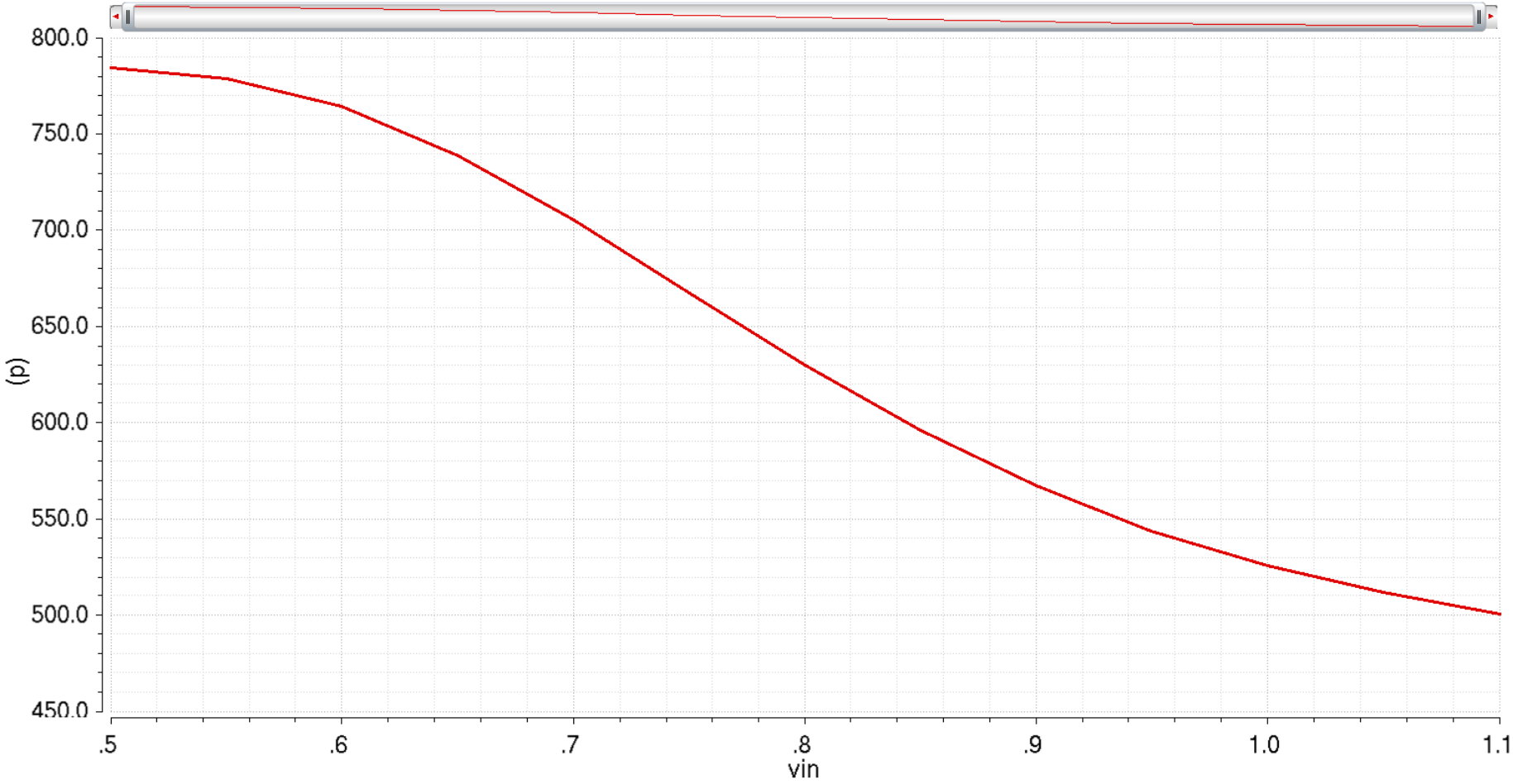
- Simple structure chosen
- Delays only rising clock edge
- Two VTC-cores in cascade



[1]



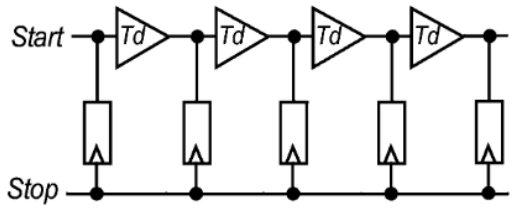
Voltage-to-Time Converter



Time-to-Digital Converter

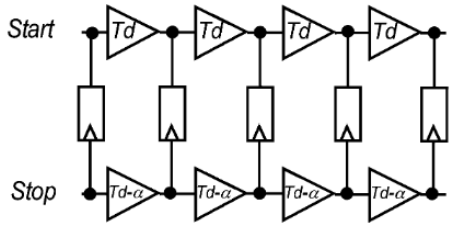
- Several architectures possible
  - Ramp TDC (with counter or ADC, but usually not high speed)
  - Delay line TDC
  - Vernier delay line TDC
  - Pipeline TDC

Delay line TDC



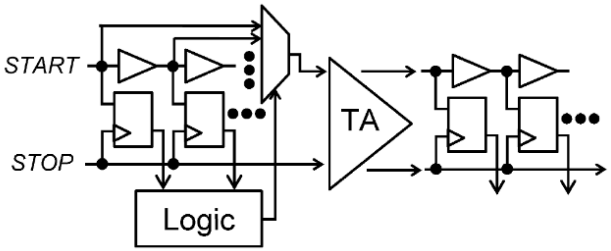
[4]

Vernier delay line TDC



[4]

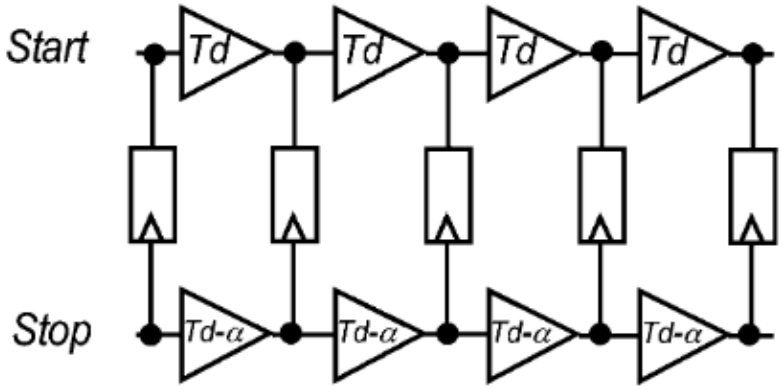
Pipeline TDC



[5]

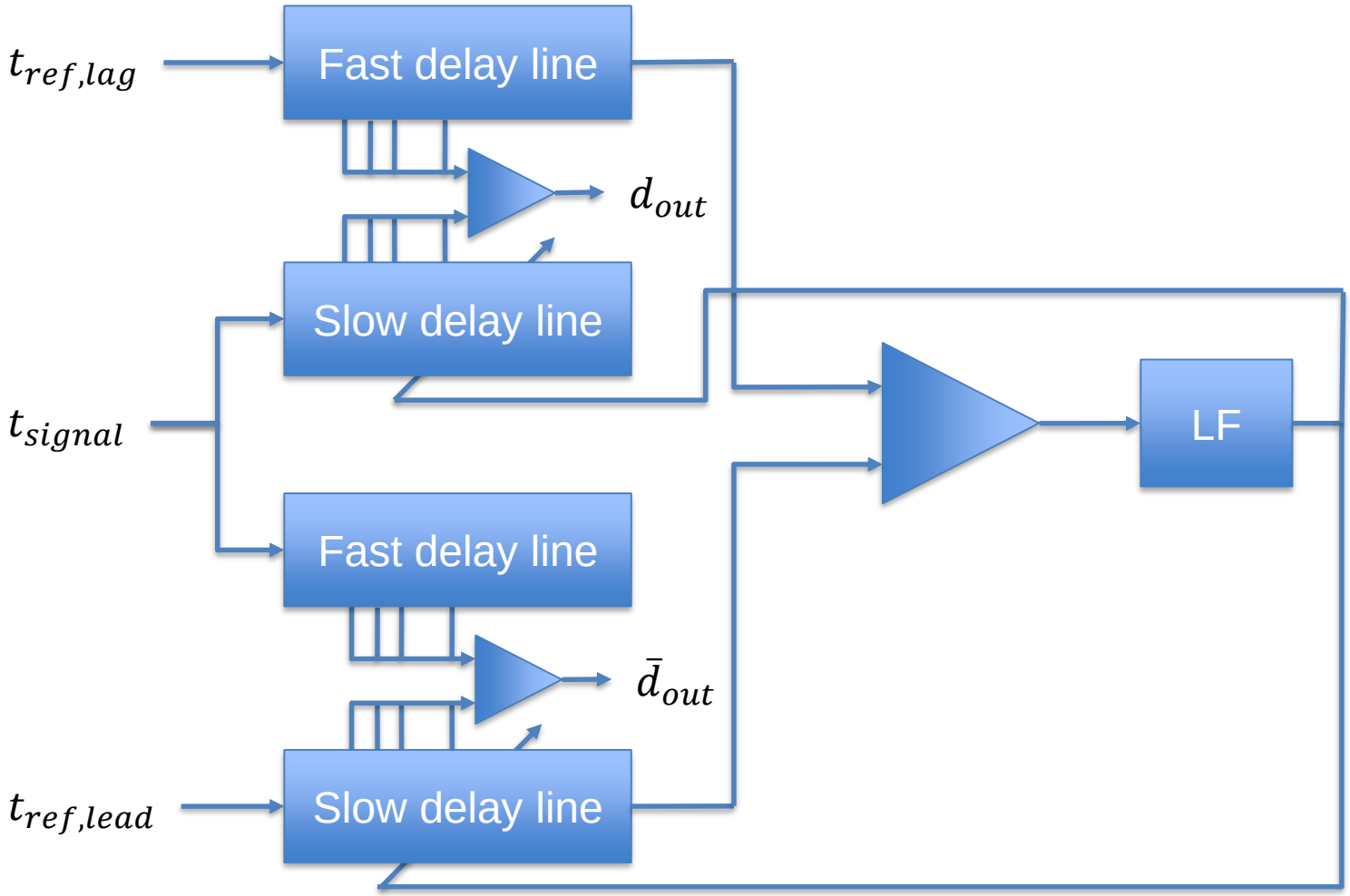
Time-to-Digital Converter

- Vernier delay line TDC chosen
  - Simple structure
  - Not limited by gate delay
- Latched pseudo comparator
- Two references (lead and lag)
- Delay locked loop to calibrate TDC to references

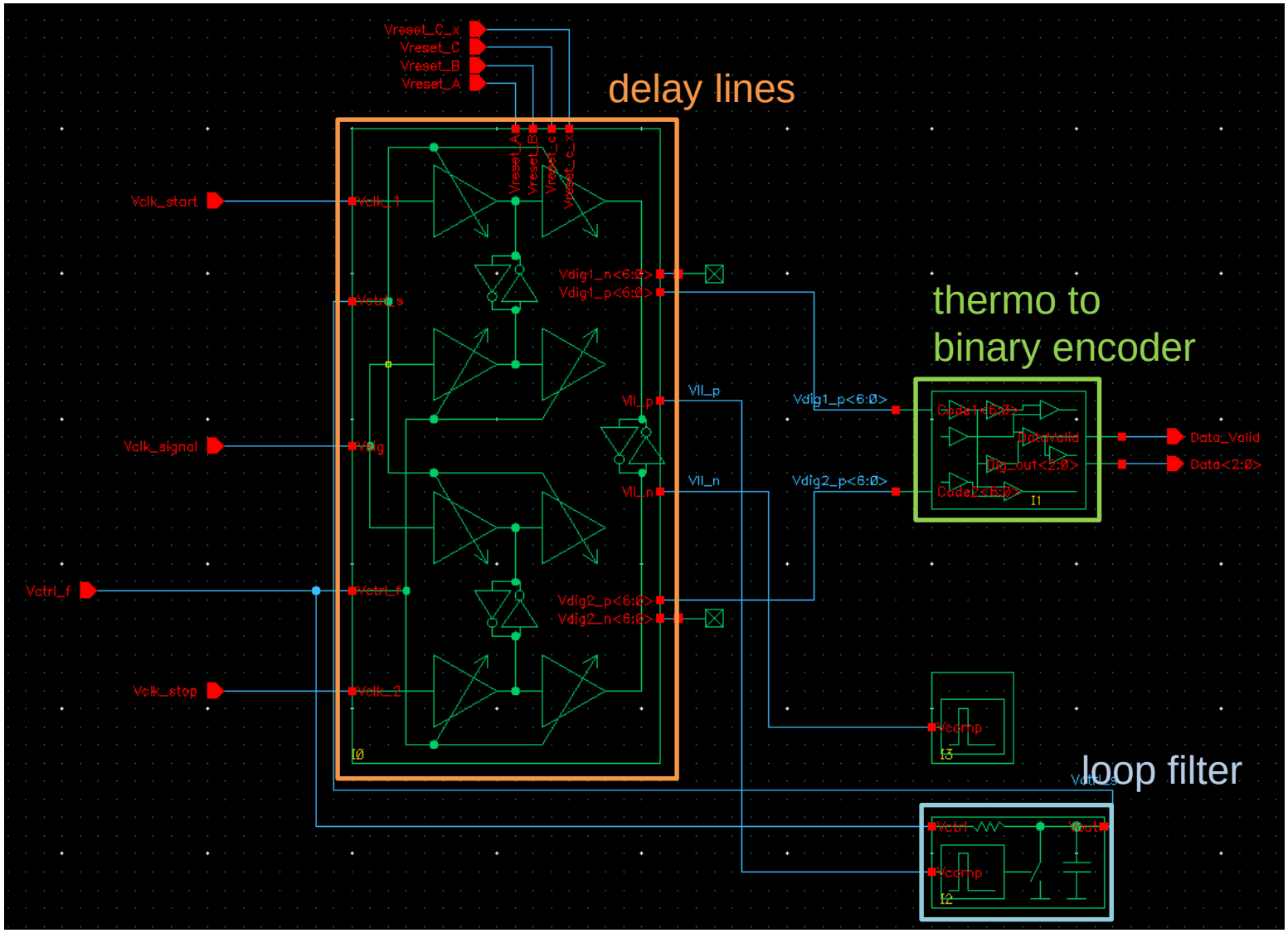


[4]

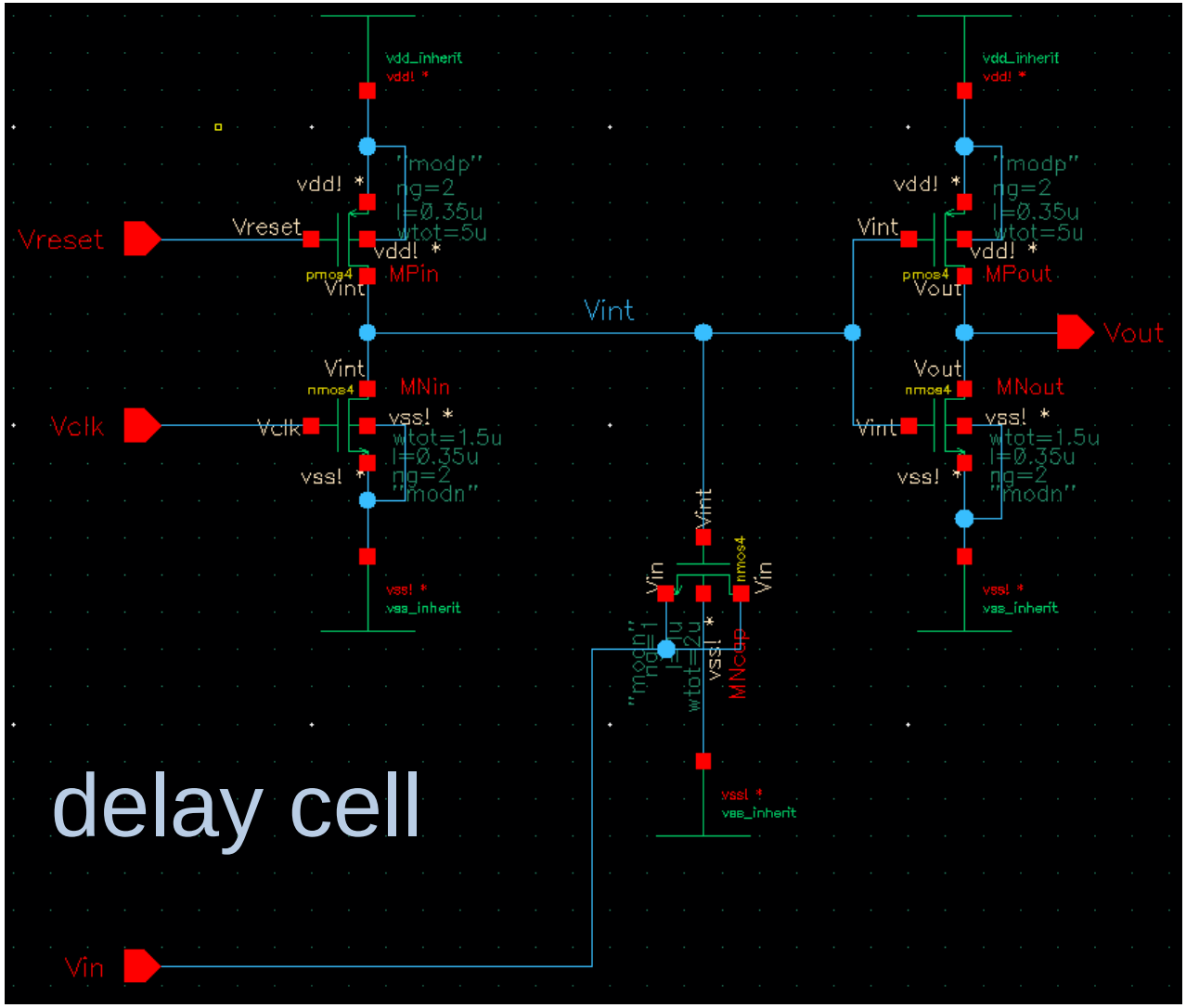
Time-to-Digital Converter



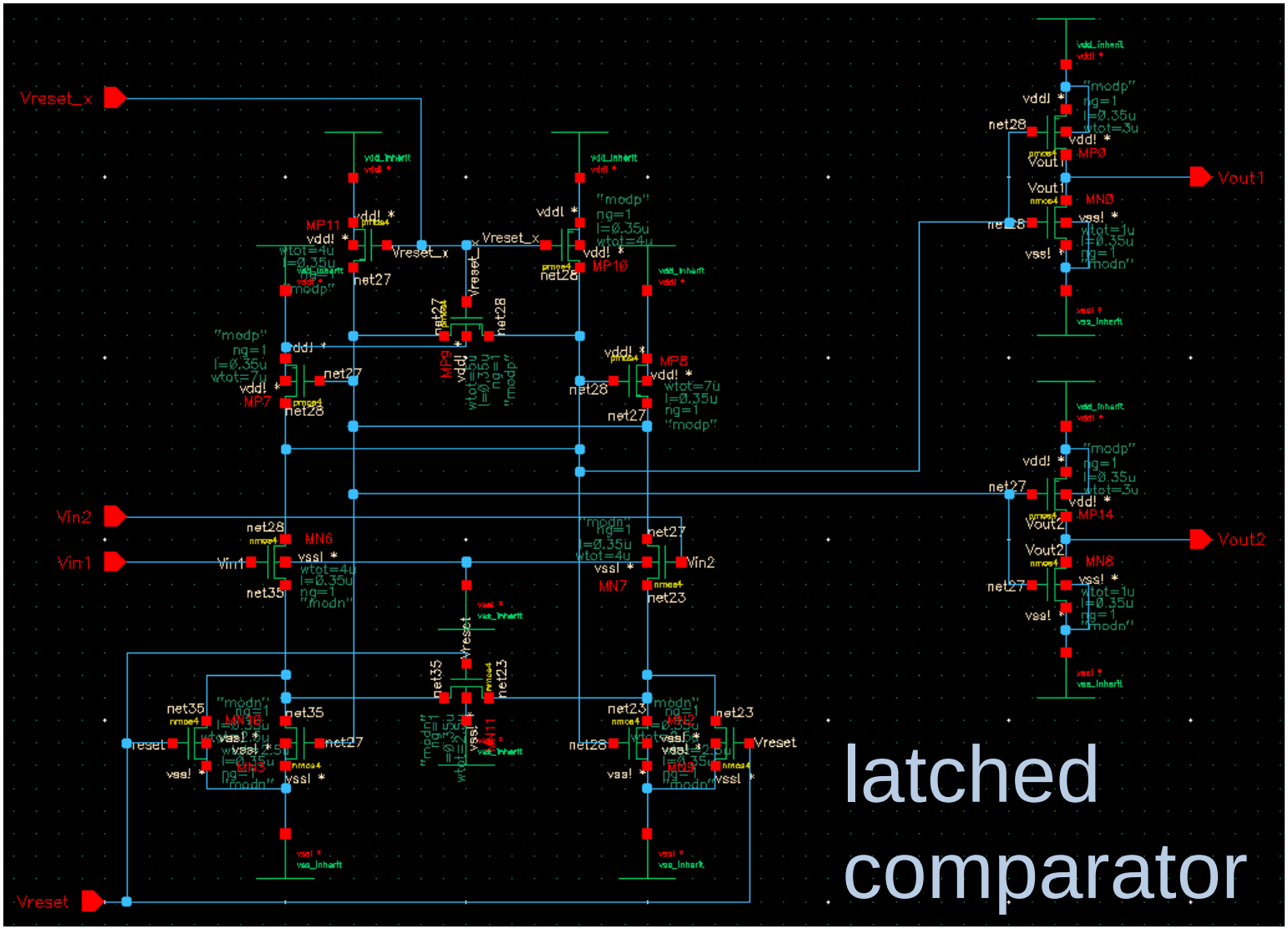
Time-to-Digital Converter



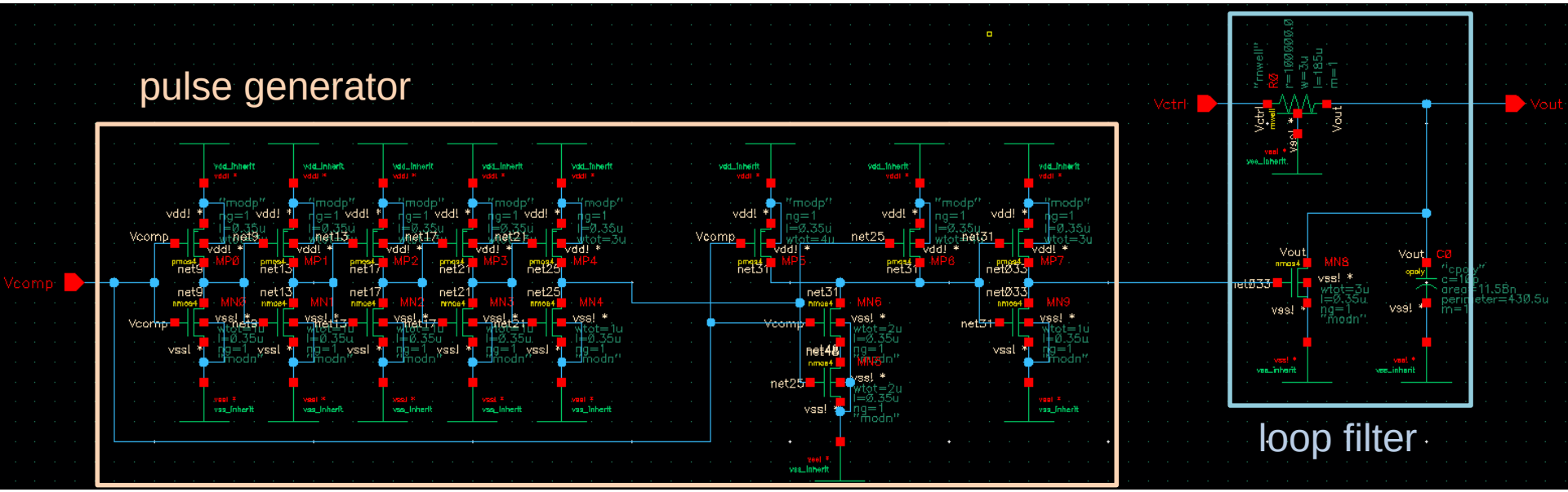
Time-to-Digital Converter



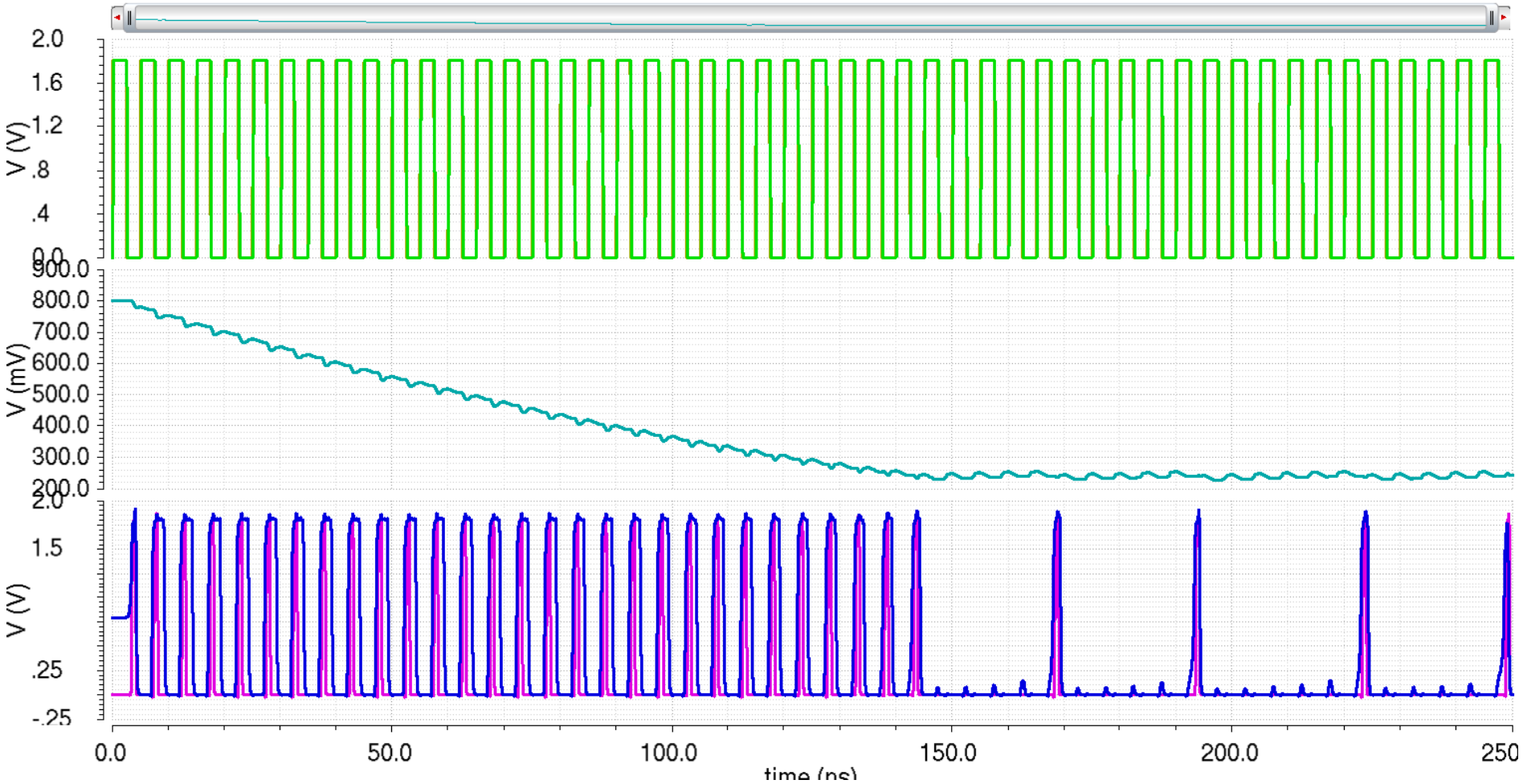
Time-to-Digital Converter



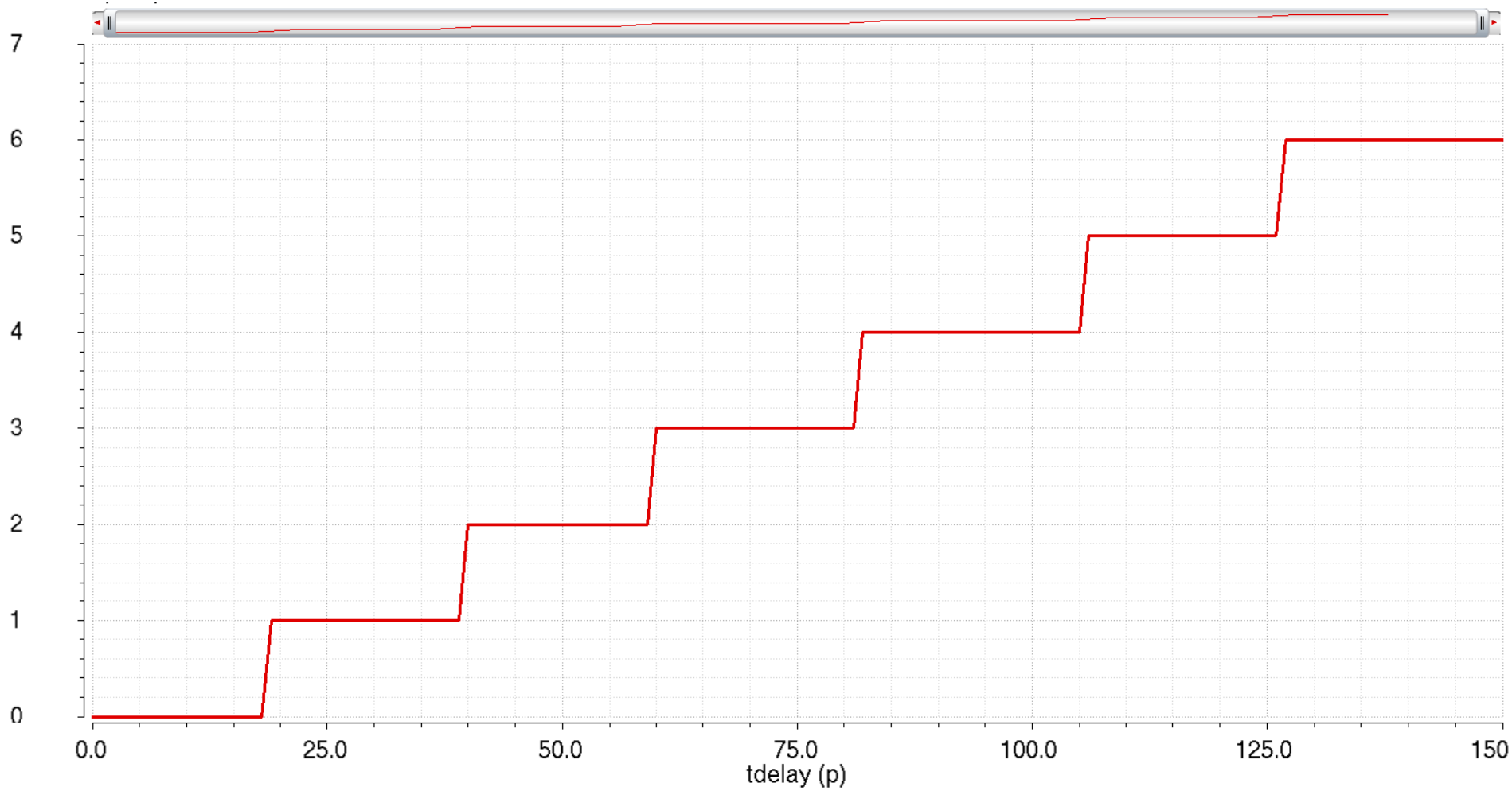
Time-to-Digital Converter



Time-to-Digital Converter

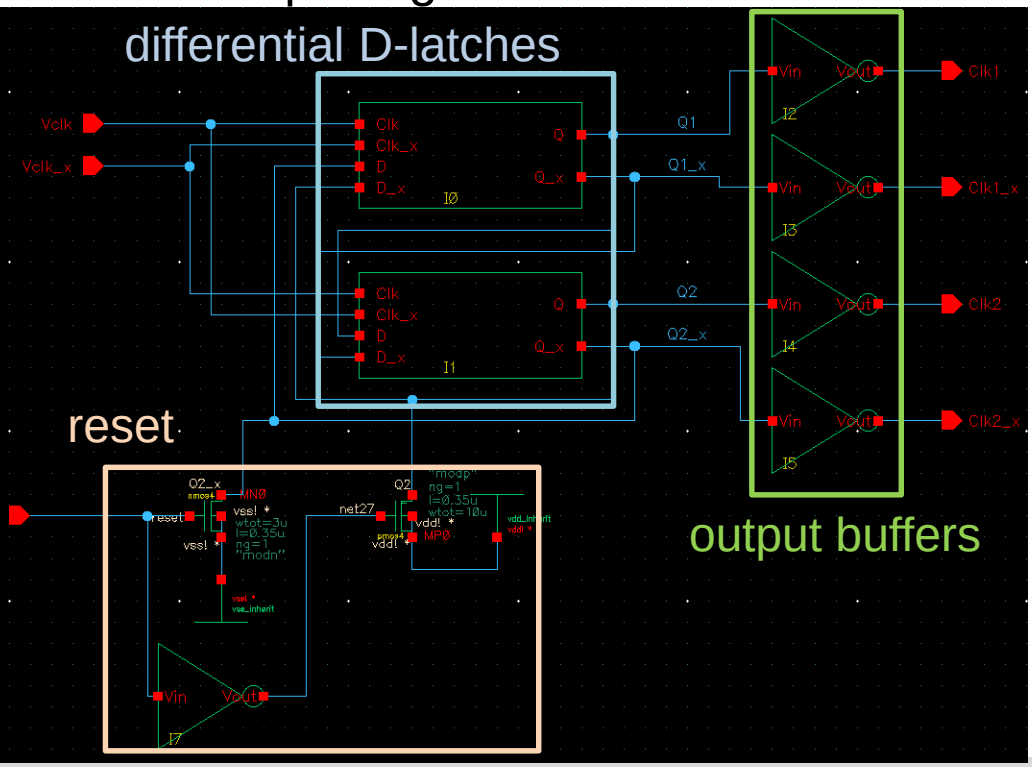


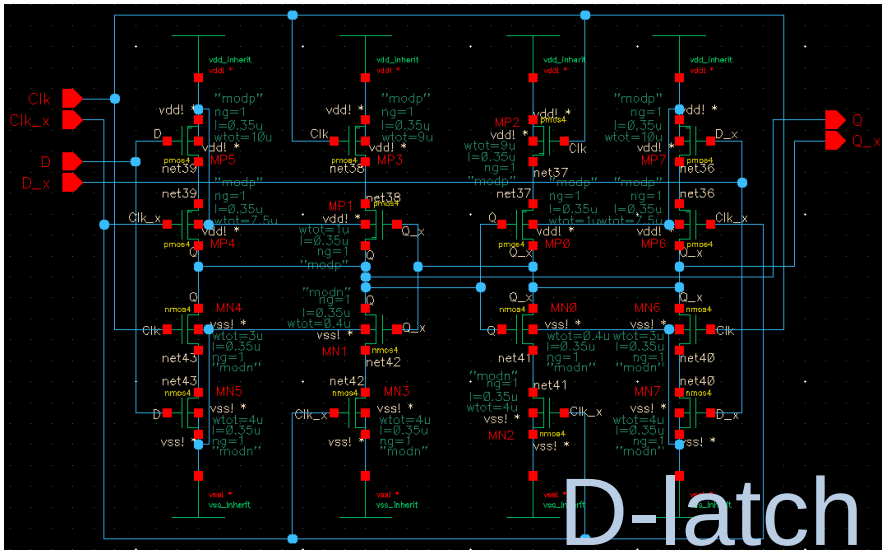
Time-to-Digital Converter



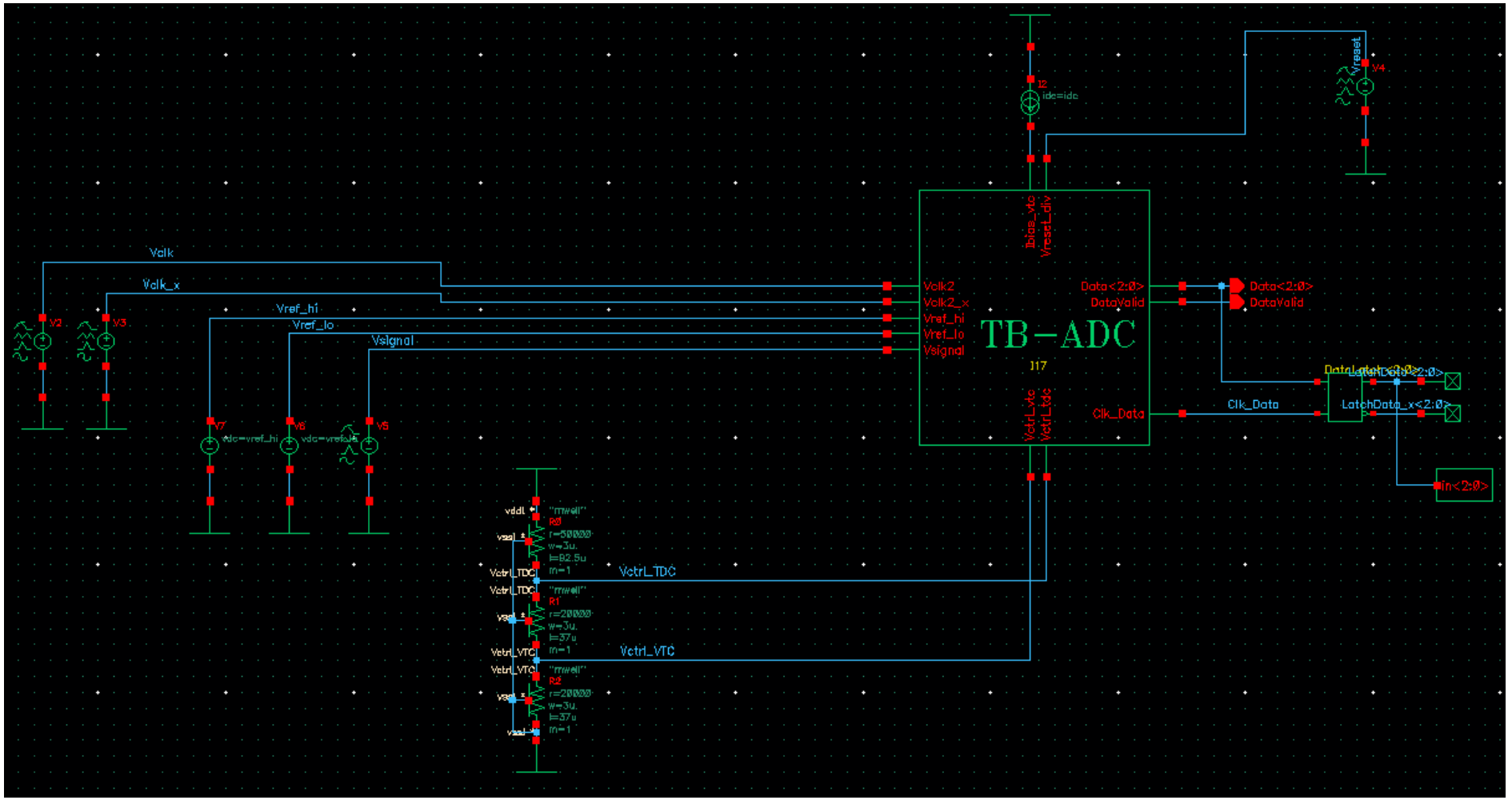
Clock Divider

- Generate I/Q clocks for reset signals of the TDC
  - Needed for 25% and 75% duty cycle signals
- Simple digital architecture

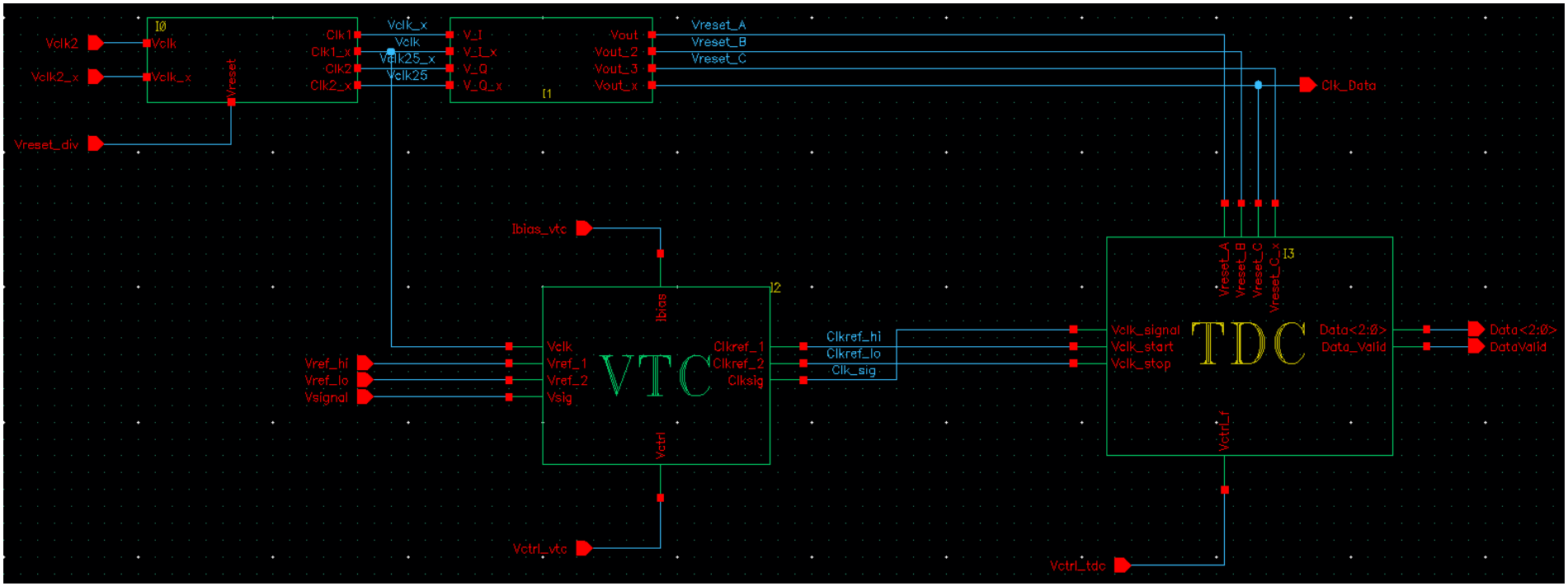




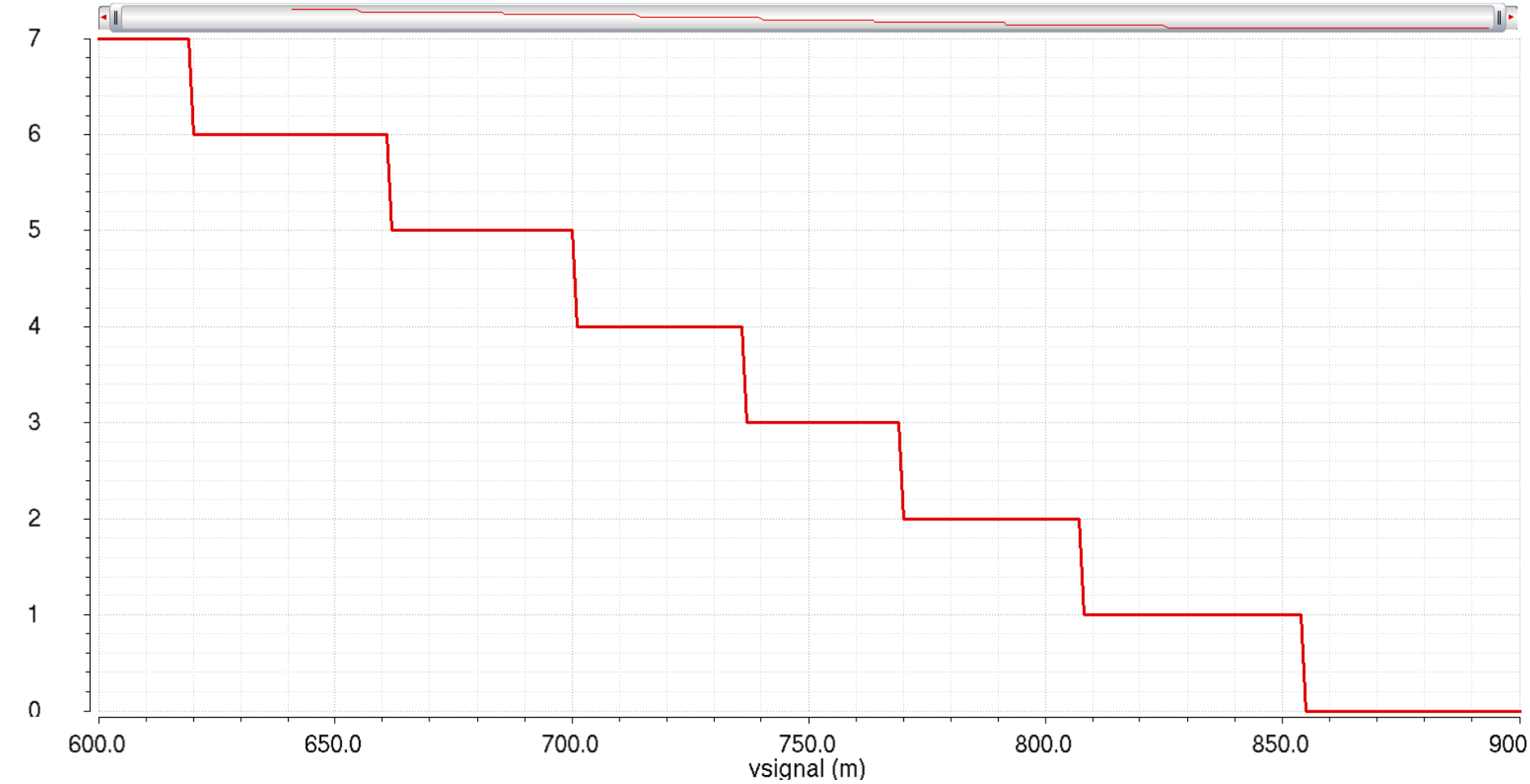
Time-Domain Analog-to-Digital Converter



Time-Domain Analog-to-Digital Converter



Time-Domain Analog-to-Digital Converter



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[5] Seon-Kyoo Lee; Young-Hun Seo; Hong-June Park; Jae-Yoon Sim, "A 1 GHz ADPLL With a 1.25 ps Minimum-Resolution Sub-Exponent TDC in 0.18 µm CMOS," in Solid-State Circuits, IEEE Journal of, vol.45, no.12, pp.2874-2881, Dec. 2010